Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A method of shifting a clock frequency of an integrated circuit device from a first frequency to a second frequency, the method comprising:
a. alternating between the first frequency and the second frequency according to a dithering pattern, said alternating occurring for a predetermined number of cycles; and
b. setting the clock frequency to said second frequency after said predetermined number of cycles.

[c2] 2.A method according to claim 1, wherein said dithering pattern gradually replaces the first frequency with the second frequency.

[c3] 3.A method according to claim 1, wherein said dithering pattern is programmable.

[c4] 4.A method according to claim 1, wherein the first frequency is a frequency of f cycles per second and the second frequency is a frequency of f/n cycles per second, wherein n is an integer.

[c5] 5.A method according to claim 1, wherein the first frequency is a frequency of f cycles per second and the first frequency is a frequency of f/n cycles per second,

wherein n is an integer.

[c6] 6.A method according to claim 1, wherein the first frequency is the same as a master clock frequency and the second frequency is said master clock frequency divided by n, wherein n is an integer.

[c7] 7.A method according to claim 1, wherein said alternating step includes:
a. providing a clock multiplexer operatively configured to select between a plurality of incoming clock frequencies, wherein the first and second frequencies are included in said plurality of incoming clock frequencies;
b. providing a dithering pattern to said clock multiplexer; and
c. selecting the first frequency or the second frequency according to said dithering pattern.

[c8] 8.A method according to claim 1, wherein said alternating step occurs at a rate of the slower of the first frequency and the second frequency.

[c9] 9.A method of shifting a clock frequency of an integrated circuit device from a first frequency to a second frequency, the method comprising:
a. providing a clock multiplexer operatively configured to select between a plurality of incoming clock frequencies,

wherein the first frequency and second frequency are amongst said plurality of incoming clock frequencies;

b. providing a dithering pattern to said clock multiplexer;

c. alternating the clock frequency of the integrated circuit between the first frequency and the second frequency according to said dithering pattern for a predetermined number of clock cycles; and

d. setting the clock frequency of the integrated circuit at the second frequency after said predetermined number of clock cycles.

[c10] 10.A method according to claim 9, wherein said alternating step occurs at a rate of the slower of the first frequency and the second frequency.

[c11] 11.A method according to claim 9, wherein the first frequency is a frequency of f cycles per second and the second frequency is a frequency of f/n cycles per second, wherein n is an integer.

[c12] 12.A method according to claim 9, wherein said second frequency is a frequency of f cycles per second and said first frequency is a frequency of f/n cycles per second, wherein n is an integer.

[c13] 13.A method according to claim 9, wherein said alter-

nating step gradually replaces said first frequency with said second frequency as the clock frequency of the integrated circuit.

[c14] 14.A system for shifting a clock frequency of an integrated circuit device from a first frequency to a second frequency, the system comprising:
a. a frequency selecting element operatively configured to switch between a first frequency input signal and a second input frequency signal, wherein said frequency selecting element provides an output frequency signal;
b. a dithering pattern control element operatively configured to produce a dithering pattern, said dithering pattern controlling said frequency selecting element so as to cause said frequency selecting element to alternate between said first and second input frequency signals for a predetermined number of cycles,
wherein said output frequency signal is set at said second frequency signal after said predetermined number of cycles.

[c15] 15.A system according to claim 14, wherein said dithering pattern control element comprises:
a. a dithering multiplexer; and
b. a latch operatively configured to store one or more dithering patterns, said dithering patterns provided to said dithering multiplexer,

wherein said dithering multiplexer is operatively configured to select between a first frequency value and a second frequency value.

[c16] 16.A system according to claim 14, wherein said dithering pattern is operatively configured to gradually replace said first input frequency signal with said second input frequency signal.

[c17] 17.An integrated circuit comprising the system of claim 14.

[c18] 18.An electronic device comprising the system of claim 14.

[c19] 19.A system according to claim 14, wherein said frequency selecting element is a multiplexer or an analog mixer.

[c20] 20.A system according to claim 15, wherein said dithering multiplexer selects at a cycle rate of the slower of said first input frequency signal and said second input frequency signal.